

Figure 1

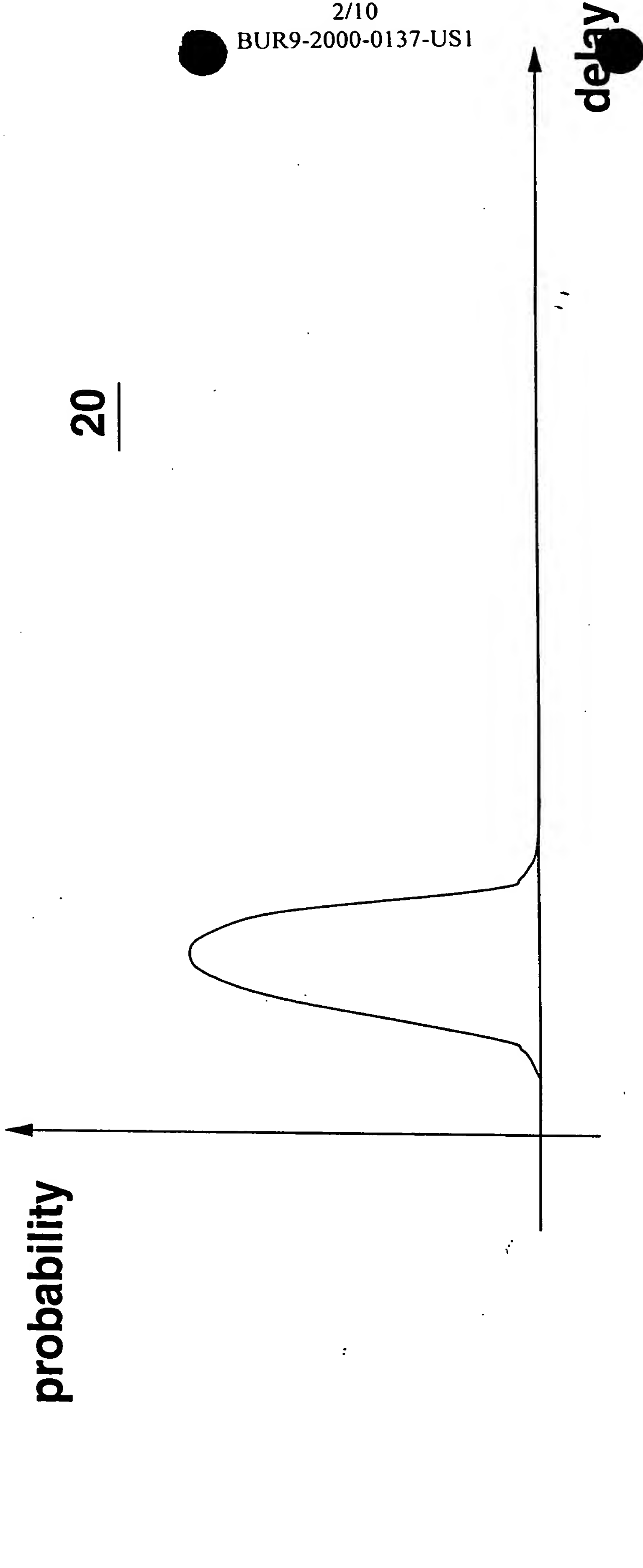


Figure 2

FIG. 3 is a graph of probability versus delay.

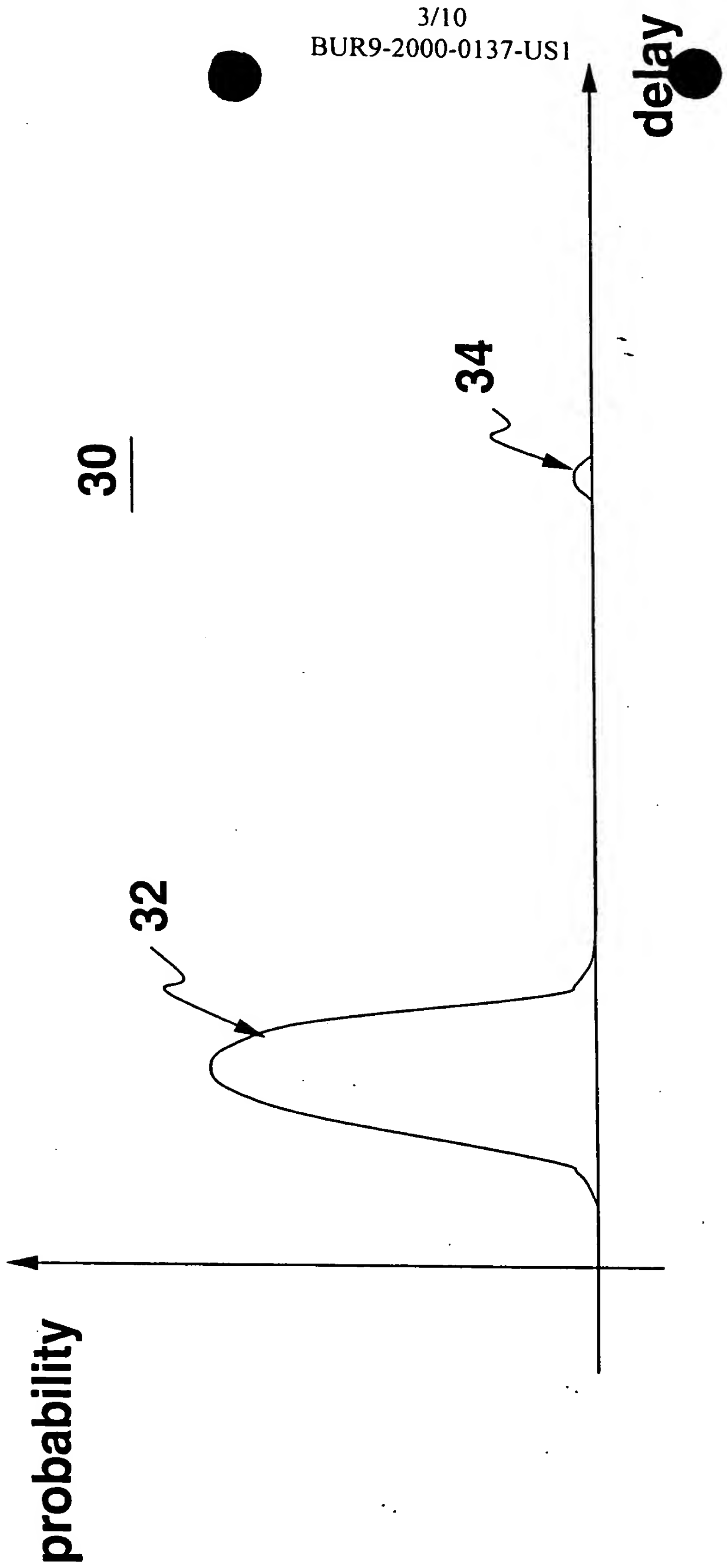


Figure 3

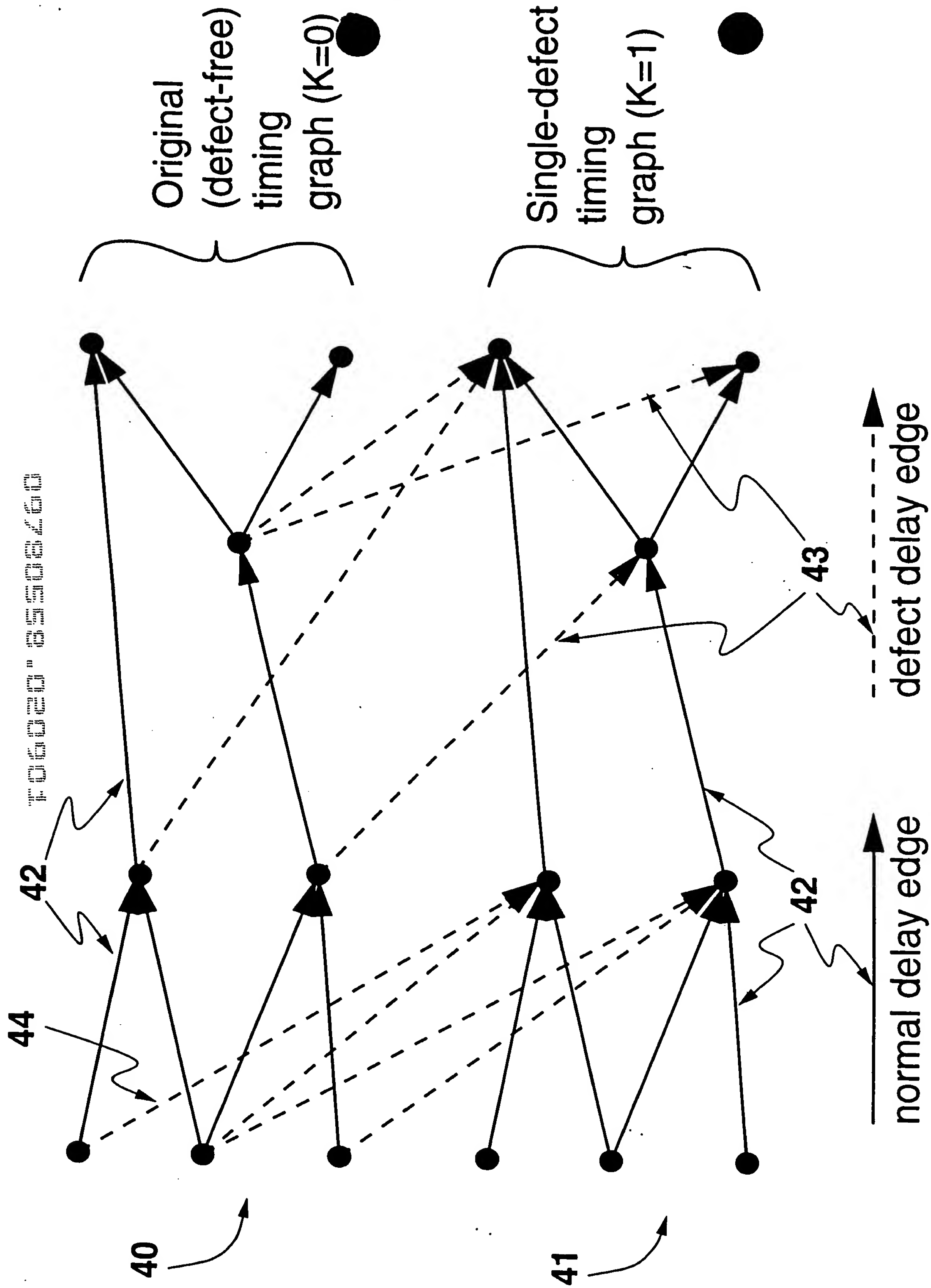


Figure 4a

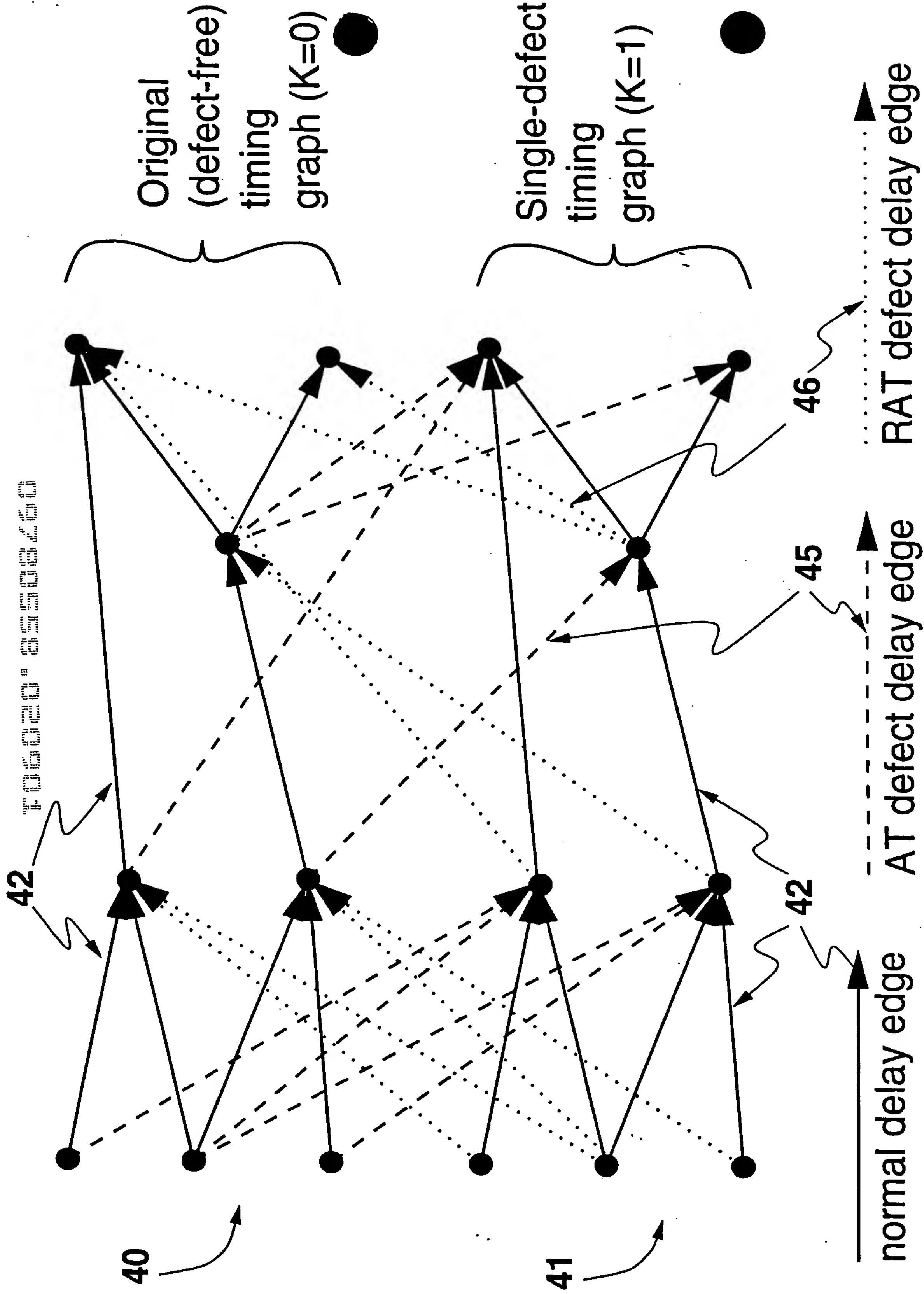


Figure 4b

50

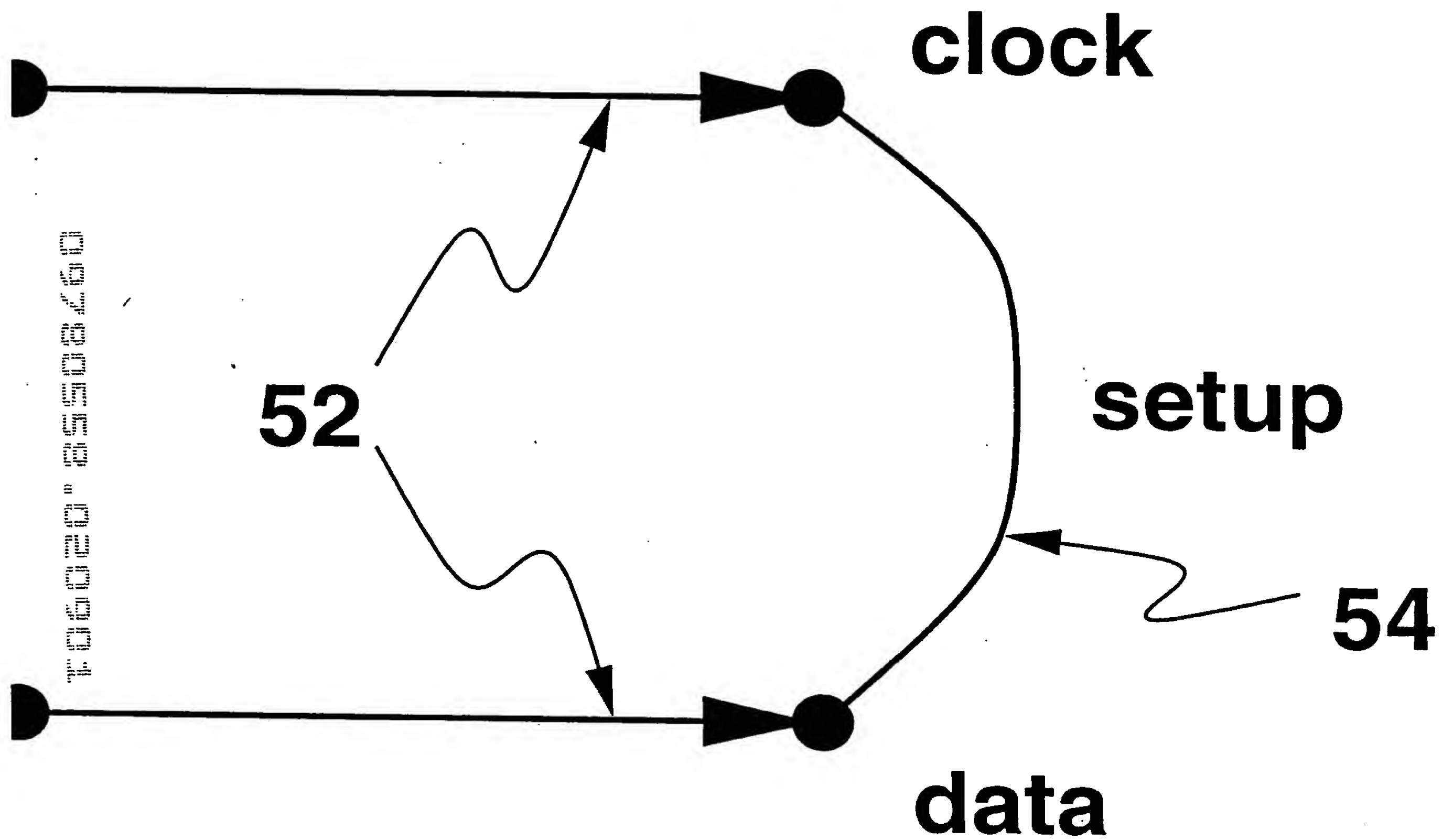


Figure 5a

clock

data

clock

setup

data

Figure 5b

1. **Содержание:** 1. Введение. 2. Описание объекта исследования. 3. Методология исследования. 4. Результаты исследования. 5. Заключение.

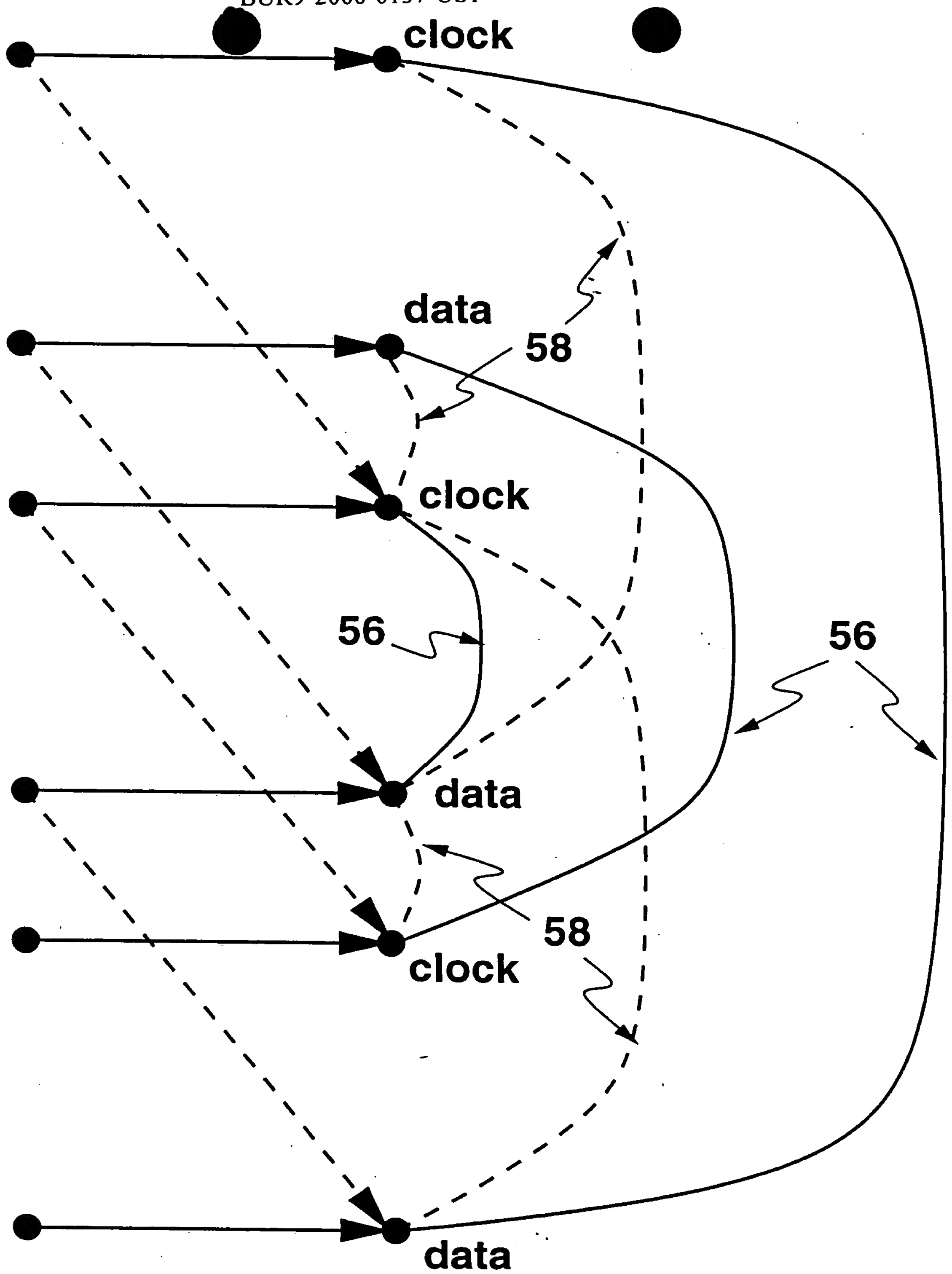
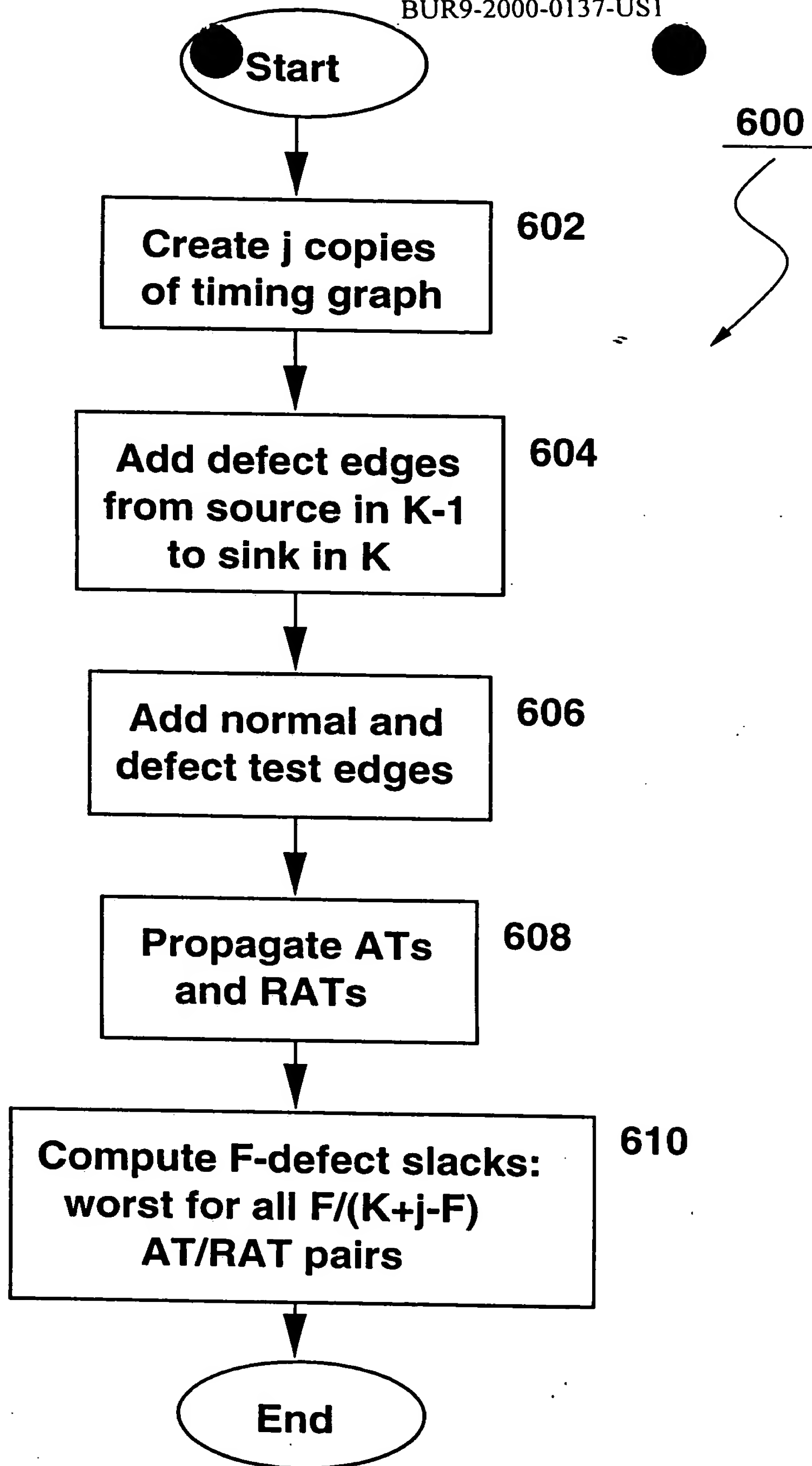
K=0**K=1****K=2**

Figure 5c

**Figure 6**

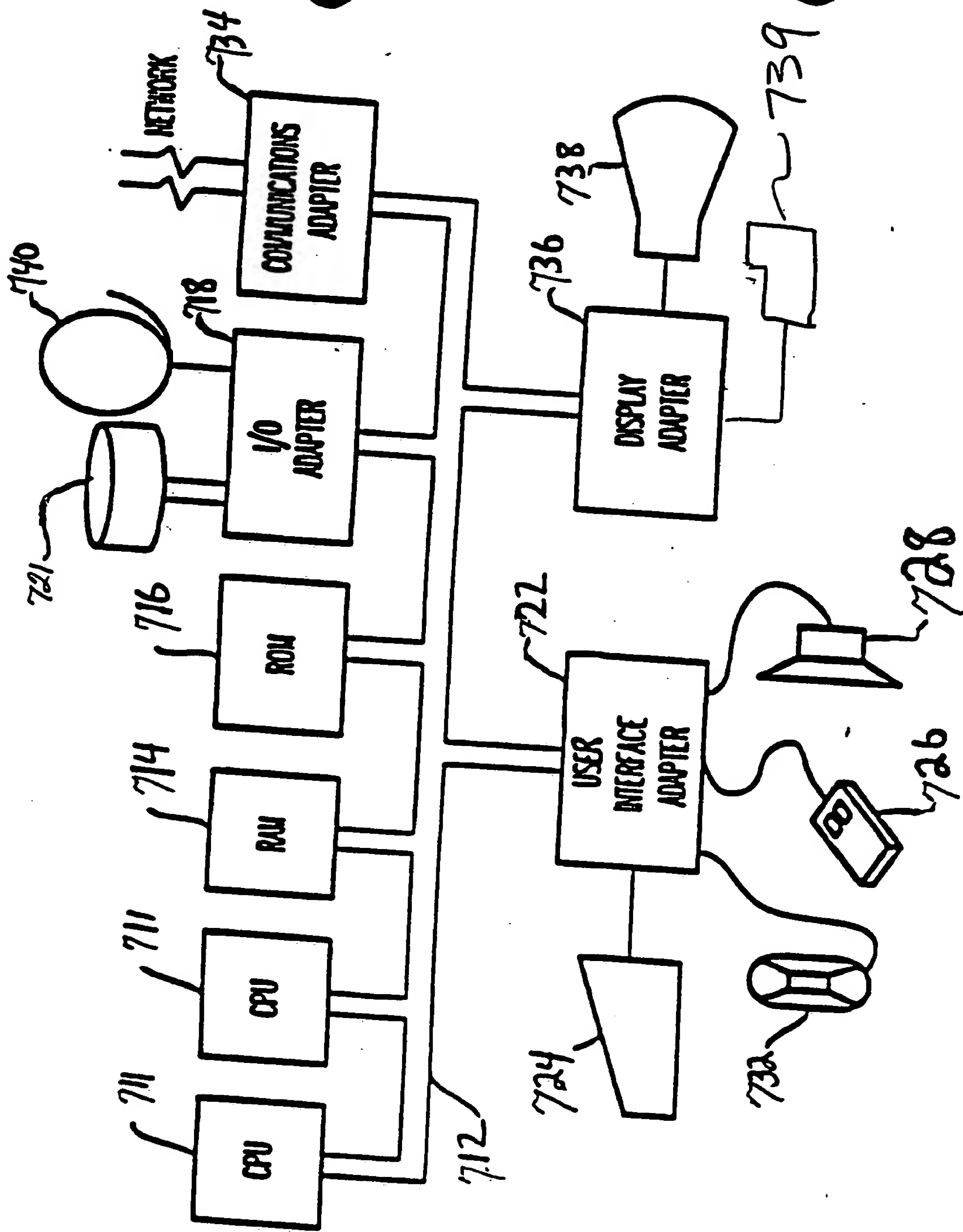


FIGURE 7

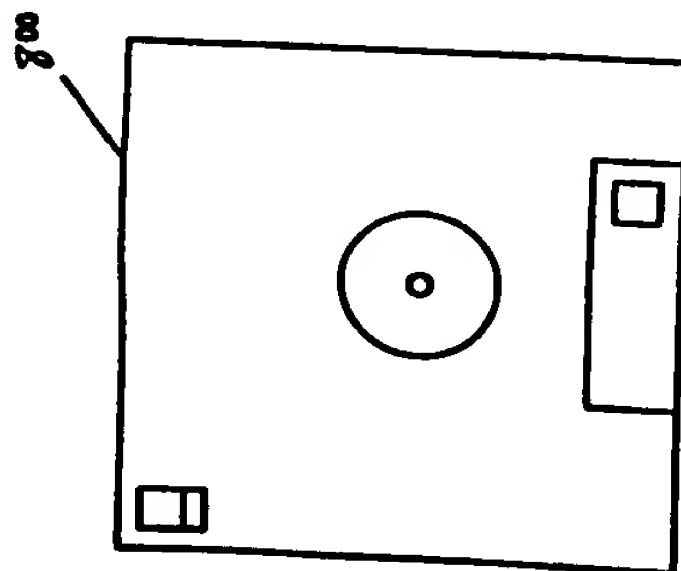


FIGURE 8